A Fundamental Step-Up Method for Standard Voltage Transformers based on an Active Capacitive High-Voltage Divider

E. Mohns, J. Chunyang, H. Badura, P. Raether

Acknowledgement: Parts of the presented work are used in the projects 17NRM01 (TrafoLoss) and 17IND06 (FutureGrid II) which have received funding from the EMPIR programme co-financed by the Participating States and from the European Union's Horizon 2020 research and innovation programme.

Full Citation of the original article published by IEEE:
E. Mohns, J. Chunyang, H. Badura and P. Raether, "A Fundamental Step-Up Method for Standard Voltage Transformers Based on an Active Capacitive High-Voltage Divider," in *IEEE Transactions on Instrumentation and Measurement*.
doi: 10.1109/TIM.2018.2880055

Available at:
https://doi.org/10.1109/TIM.2018.2880055

A Fundamental Step-Up Method for Standard Voltage Transformers based on an Active Capacitive High-Voltage Divider

E. Mohns, J. Chunyang, H. Badura, P. Raether

***Abstract*—This paper presents the new fundamental step-up method for standard voltage transformers at PTB, as well as the setup of the required components. A main component is an active low-voltage capacitor, designed to realize capacitive voltage dividers by means of compressed–gas, high-voltage capacitors for rated primary voltages between 5 kV and 800 kV / √3. This divider has a negligible voltage dependency and low phase errors at 50 / 60 Hz. Using the other components, mainly a two-stage voltage transformer with integrated inductive voltage divider and a sampling-based voltage comparator, a transfer uncertainty for one build-up step of below $1 \cdot 10^{-6}$ ($k = 2$) has been reached.**

***Index Terms*—Voltage transformer, capacitive divider, high voltage, inductive voltage divider, uncertainty, ratio error, phase displacement.**

I. Introduction

At the Physikalisch-Technische Bundesanstalt (PTB), the measurands "ratio error" and "phase displacement" for voltage transformer (VT) calibration in the voltage range from 1 kV to 800 kV / √3 at 50 Hz and 60 Hz are maintained in a 1000 V inductive voltage divider (IVD), a set of six different standard VTs whose accuracy class is 0.02 or better and a voltage transformer bridge [1], which is directly connected to the standard VT and the VT under test. In contrast to the widely used calibration method for VTs, using capacitors as sensing elements [2] and a current comparator-based bridge [3], the use of these inductive standard transformers as reference ensures excellent long-term stability without verifying it prior to the calibration of a VT under test. From time to time, it is necessary to determine the ratio errors and phase displacement of all VTs via a fundamental step-up method, e.g. in [4], which reflects the state of the art. The new step-up method for transferring the accuracy of the VT(n-1) with known errors to the VT(n) to be calibrated is shown Fig. 1. As transfer standard a capacitive voltage divider (CVD) is used due to its potential high linearity, i.e. only small scale factor changes occur with varying input voltages, while its phase error remains almost constant.

In Step I) a CVD is calibrated at the lower primary voltage U_{P1} by using VT(n-1) and a precise hybrid voltage transformer VT_H, with adjustable nominal ratio. The voltage comparator determines the complex voltage ratio $\underline{U}_2 / \underline{U}_1 = \underline{\Gamma}_{21}(I)$ in this step (I) in order to determine the output-to-input ratio of the CVD $\underline{F}_{CVD} = \underline{U}_2 / \underline{U}_P$ based on the ratio $\underline{F}_N(n\text{-}1) = \underline{U}_S / \underline{U}_P$ and $\underline{F}_H(I) = \underline{U}_1 / \underline{U}_S$ of the standard VT(n-1) and the auxiliary VT_H. The ratio of the CVD is $\underline{F}_{CVD} = \underline{\Gamma}_{21}(I) \cdot \underline{F}_N(n\text{-}1) \cdot \underline{F}_H(I)$.

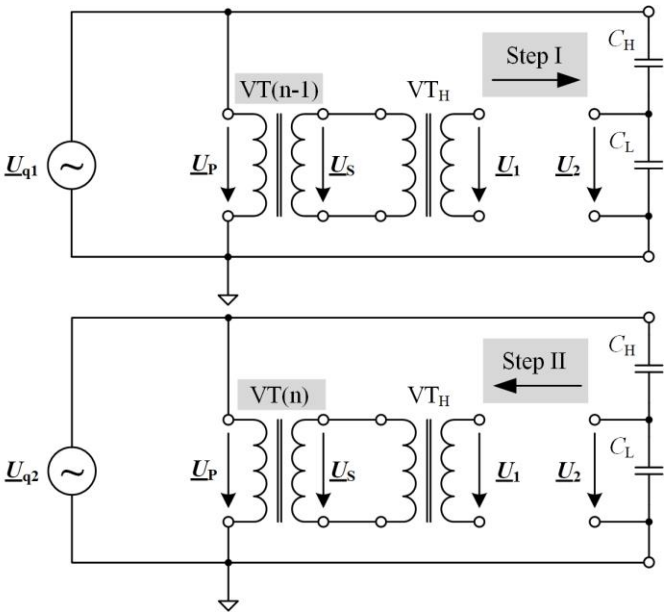

Fig. 1. Two-Step realization of a step-up calibration of a VT(n) using a capacitive voltage divider, a known VT(n-1), an auxiliary VT_H and a sampling based voltage comparator.

In the second step (II), VT(n-1) is replaced by VT(n). Assuming, that the CVD has negligible ratio drift and a negligible voltage dependency, the ratio $\underline{F}_N(n) = \underline{F}_{CVD} / (\underline{\Gamma}_{21}(II) \cdot \underline{F}_H(II))$ of the VT(n) can be calibrated at the higher voltages U_{P2} by substituting $\underline{F}_{CVD}$ of the previous step

$$\underline{F}_N(n) = \underline{F}_N(n\text{-}1) \cdot \frac{\underline{\Gamma}_{21}(I)}{\underline{\Gamma}_{21}(II)} \cdot \frac{\underline{F}_H(I)}{\underline{F}_H(II)} \quad (1)$$

The VTs ratio error ε_U and the phase displacement δ_U can be calculated from the definition $\underline{F}_N = (1 + \varepsilon) / K_N \cdot e^{j\delta}$. In order to

This paper was submitted for review on 8. July 2018.

E. Mohns, H. Badura and P. Raether are with the Physikalisch-Technische Bundesanstalt, Bundesallee 100, 38116 Braunschweig, Germany (e-mail: enrico.mohns@ptb.de).

J. Chunyang is with the China Electric Power Research Institute, Luoyu Road 143, 430074 Wuhan, China.

carry out step-up calibrations according to this procedure, with low transfer uncertainties in the order of ppm or µrad, several aspects on the main components of this step-up method have to be considered. The main components are the CVD, a hybrid voltage transformer and a sampling-based voltage comparator. In the following, these components, their setup and their measurement results are presented and discussed.

II. Setup of the Components

A. Active Capacitive Voltage Divider

The CVD design shall have a high short-term ratio stability for the duration of one cycle of the step-up calibration (around 20 minutes), a negligible voltage dependency as well as stable and low phase errors. For the high-voltage arm of the CVD, PTB has several compressed–gas, high-voltage capacitors with voltage ratings from 120 kV to 800 kV and capacitance values of C_H = 100 pF (120 kV), 50 pF (500 kV) and 70 pF (800 kV). Their individual voltage dependencies are known [5] and their loss factors (tan δ) are within 10^{-5}. Therefore, the focus is on the setup of the low-voltage arm of the CVD. The principle of the active CVD is shown in Fig. 2. It is based on an inverting structure [6], where the high-voltage capacitor C_H is connected via a coaxial cable to the current input of the active low-voltage capacitor (ALVC), made up by the capacitor C_L and an operational amplifier (OPA). In order to allow the adjustment of all required scale factors for the lowest primary voltage as well as for the highest primary voltage of the standard VT set, the ALVC comprises of several selectable capacitors from C_L = 100 nF to 7.4 µF with increments of 100 nF [7].

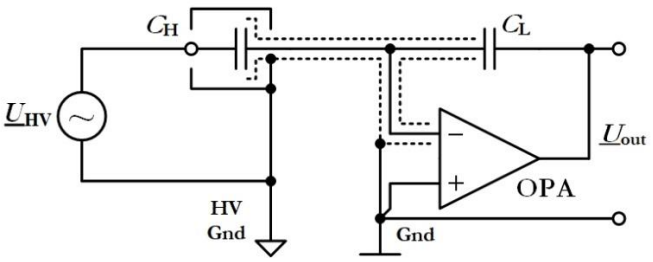

Fig. 2. Principle of the active capacitive divider.

Assuming an ideal OPA with infinite loop gain and taking the individual phase displacements δ_H and δ_L of C_H and C_L to 90 ° into account, the voltage ratio $\underline{F}_{CVD}$ of the CVD is

$$\underline{F}_{CVD} = \frac{\underline{U}_{out}}{\underline{U}_{HV}} = -\frac{\underline{Z}_L}{\underline{Z}_H} = -\frac{C_H}{C_L} \cdot e^{-j(\delta_L - \delta_H)} \quad (2)$$

The maximum output voltage chosen for the CVD is within the input voltage range of 10 V_{pk} of a two-channel sampling system [8], which can handle the phase shift of 180 ° of the CVD. Assuming a 5V_{rms} output, scale factors can be realized from 5kV / 5V (100nF / 100pF) to 550kV / 5V (7.4µF / 70pF) using just one active LV capacitor. The maximum capacitive current is around 10 mA at 50 Hz. The setup of the low-voltage arm as an inverting amplifier has the advantage that both capacitors C_H and C_L are operated according to the definition (i.e., the Lo terminals are at virtual ground potential) and, due to the use of a coaxial cable connected to the HV capacitor, there is no substantial sensitivity against pick-up noise or the cable capacitance. Furthermore, the output can be loaded with the sampling system without changing the divider's ratio or phase. However, several other aspects must be considered as well: (i) type of the capacitor in use and their arrangement; (ii) finite open-loop gain of the OPA; (iii) leakage of the printed circuit board (PCB) or due to non-negligible resistance of the switches or to the critical tracks of the PCB; and (iv) DC feedback for the operational amplifier (OPA).

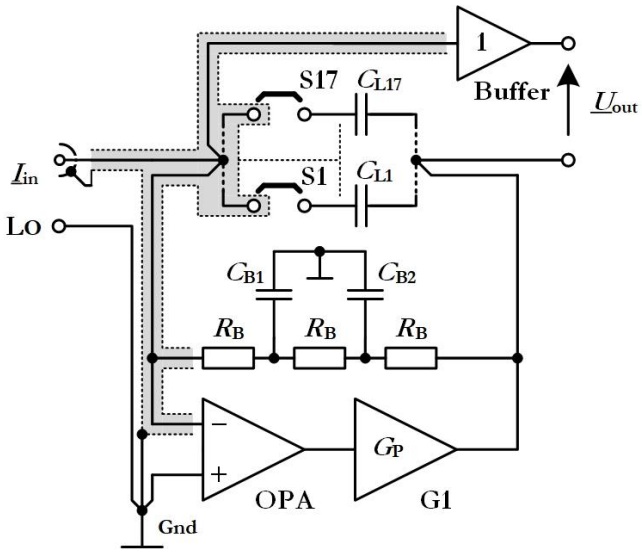

Fig. 3. Scheme of the active LV capacitor.

The scheme of the ALVC, which overcomes most of these aspects, is shown in Fig. 2. Due to the high capacitance values which have to be realized, ceramic capacitors with NP0 temperature characteristics have been chosen due to their low temperature sensitivity and their low dissipation factor, which are in the order of 10^{-5} and their high long-term stability [9], [10], [11]. Seventeen capacitors C_{L1} to C_{L17} can be individually switched in parallel, from which fourteen are made of 500 nF capacitors, two are made of 100 nF capacitors and one is made of a 200 nF capacitor. All of the capacitors were realized from one batch of 100 nF SMD capacitors (NP0) with a voltage rating of 100 V (size 1812). An initial measurement of a single 100 nF capacitor has shown a voltage dependency of about 70 µF / F at 100 V_{rms} with a square law characteristic, so that for a maximum output voltage of the ALVC of 7 V_{rms}, a dependency of 0.4 µF / F can be extrapolated. To decrease this voltage dependency to about one quarter (i.e. to 10^{-7}), four single capacitors of 100 nF, properly connected in a parallel-series configuration form a single capacitor block of 100 nF with a voltage rating of 200 V. The nominal values of 200 nF and 500 nF were realized from stacking several of such capacitor block of 100 nF blocks in parallel. In total about 300 capacitors were used for the ALVC, so that matching of each capacitor value of C_L to within 0.5 % could be realized.

The defining sense points of C_L are located at C_{L8}, i.e. in the middle between C_{L1} and C_{L17}. The output "Lo", connected via the FET buffer amplifier, as well as the output "Hi" are

connected to these defining "sense points". This semi-differential output ensures highest possible accuracy in case of the inverting amplifier structure with finite gain OPA. The use of a driver stage G_P within the feedback loop of the low-noise FET OPA has some advantages, besides the obvious fact, that the current through C_L is driven from G_P. The gain of G_P in the low audio frequency range up to 16 kHz is set to 20 dB, while at high frequencies it is set to 0 dB in order not to decrease the loop stability. Additionally, a low Q notch filter with a tuning frequency of 53 Hz was implemented, leading to an extra gain of 30 dB around 50 / 60 Hz. The maximum output current of G_P is 250 mA_{pk}. This opens the use of this ALVC in the future for measurements with distorted waveforms or even at higher frequencies too.

To keep the additional tan δ loss due to the series resistance of the relevant PCB tracks as low as possible, they are made as low resistive as practically possible. The switches S1 to S17 take place via low-resistance connection plugs (several mΩ). A low leakage has been obtained using a PCB laminate with low leakage (RO4350B) and using proper grounded guard structures (see grey-shaded area in Fig. 3) around the inverting input as well as around the two poles of the connection plugs. Several vias in the guard structure from the top layer to the bottom layer additionally lower potential leakage through the PCB laminate by providing a sink to ground. A further reduction of leakage has been achieved by omitting the area in the PCB laminate directly under the capacitors.

The bootstrap circuit, which is realized as a two-stage network with R_B, C_{B1} and C_{B2} ensures a DC bias path for the OPA, while the equivalent parallel impedance at frequencies higher than the pole frequency ($1/R_BC_B$) becomes extremely high and is about $\omega^2 R_B^3 C_{B1} C_{B2}$. With the chosen values of R_B = 3.9 MΩ, C_{B1} = 0.15 µF and C_{B2} = 0.1 µF, the equivalent parallel impedance is in the order of 100 GΩ at 50 Hz. This, in turn, leads to an additional tan δ of below $3 \cdot 10^{-7}$ at 50 Hz, even with the smallest C_L of 100 nF. All these measures ensure that the tan δ for all combinations of C_L in use are practically equal and are also equal to the tan δ of an individual capacitor.

Care has been taken to obtain an optimized low frequency settling (transient phenomenon). Simulation show that an optimal-damped settling is obtained by choosing C_{B1} = 1.5 C_{B2}. For C_L = 100 nF, the settling time is about 5 s. Due to the large range of adjustable capacitances C_L from 100 nF to 7 µF, two bootstrap circuits have been implemented.

B. Hybrid Voltage transformer for Scaling

The fundamental task of the hybrid voltage transformer VT_H is to adapt precisely the output voltages of the standard voltage transformers VT(n-1) and VT(n) in the two steps of the step-up method to the voltage input of the voltage comparator (see Fig. 1). For obtaining highest possible transfer accuracy according to (1), the ratios F_H(I) and F_H(II) of VT_H are adjusted for getting approximately equal voltages $\underline{U}_1$ of VT_H and $\underline{U}_2$ of the CVD. The set range of VT_H shall vary from at least 100 V / 1 V (F_H = 0.01) to 100 V / 10 V (F_H = 0.1). Figure 4 shows the winding configuration of VT_H. It is based on the combination of a two-stage voltage transformer with a ratio of K_n = 10, and an integrated adjustable inductive voltage divider [8], that has one decade and one octad.

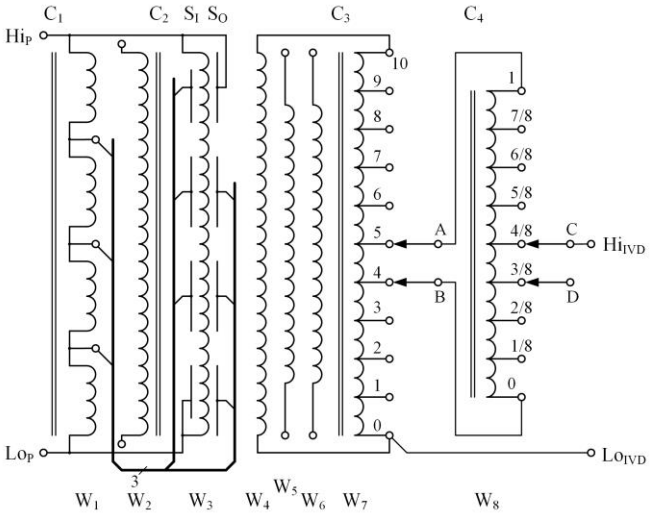

Fig. 4. Scheme of the winding configuration of the two-stage hybrid voltage transformer. The ratio is shown exemplarily for 0.045.

The inner working core, C1, which is made of nanocrystalline material [12], comprises the primary winding W1 (4 x 400t) and an auxiliary winding W2 (8 x 16t). The maximum voltage is 320 V at 50 Hz, while the maximum core impedance is 700 kΩ to prevent loading effects to VT(n) or VT(n-1). A set of four cores as a shell around this makes up the magnetic core for the second stage, C2. The primary winding of the second stage, W3, is wound in four sections (4 x 400t) and four layers to allow the use of enamelled copper wire with sufficient thickness. The four sections of W3 are shielded inside and outside by means of eight screens $S_{I,k}$ and $S_{O,k}$ (k = 1… 4), which can be driven from W1 with the accessible potentials (0 %, 25 %, 50 %, 75 % and 100 %). This minimizes capacitive leakage of W3, caused by its stray capacitances. The secondary winding W4 (160t), which has a ratio of 0.1, and two auxiliary windings, W5 (16t) and W6 (2t), which have a ratio of 0.01 and 0.00125, are wound around W3. Finally, the core, C3, and its windings, W7 (10 × 16t) and W8 (8 × 2t), represent an inductive voltage divider that is connected to the secondary winding, W4. Thus, ratios from 0.0 to 0.10 with a resolution of 0.00125 (1 / 800) can be adjusted. The purpose of the auxiliary windings, W5 and W6, is to allow the IVD section to be calibrated using Thompson's method [16]. The voltage ratio of the VT_H, which is the cascade of the VT section and the IVD section, can be expressed by

$$\underline{F}_H = \frac{1+\varepsilon_{VT}+j\,\delta_{VT}}{K_n} \cdot \left(D_n + \alpha_{IVD} + j\,\beta_{IVD}\right) = D_H \cdot (1+\varepsilon_H) \cdot e^{j\delta_H}, \qquad (3)$$

where K_n is the transformer ratio, ε_{VT} and δ_{VT} are the ratio error and the phase error of the VT section, D_n is the nominal divider ratio, and α_{IVD} and β_{IVD} are the in-phase and quadrature corrections of the IVD section. Note the different error definitions, where the transformer errors are related to its secondary output voltage (RTO), while the divider corrections are referred to the divider input voltage (RTI). The whole

voltage ratio of VT_H can be described by one common divider ratio $D_H=D_n / K_n$ as well as the combined ratio error $\varepsilon_H = \varepsilon_{VT} + \alpha_{IVD} / D_n$ and the phase error $\delta_H = \delta_{VT} + \beta_{IVD} / D_n$. To calibrate VT_H, the VT section and the IVD section has to be calibrated separately. For this purpose, the secondary output as well as the output of the first IVD decade (points A, B) and the output of the second IVD octad (points C, D) are separately accessible via connector plugs on the front panel.

By choosing reasonable low primary winding resistances R_{P1} and R_{P2}, and high magnetic core impedances $\underline{Z}_{M1}$ and $\underline{Z}_{M2}$ of the first and of the second stage, the excitation error of the VT section is theoretically below 10^{-8}. In practice, effects due to stray magnetic fields around the cores and capacitive effects will occur and deteriorate the given estimated error. To obtain an IVD section with low errors, the first decade (W7) is wound in 10 layers of copper wire with PTFE insulation of 16 turns. To obtain high symmetry, a 3 D printed winding support with 16 uniformly spaced thin sections (slots) for the 10 layers is used. The layers in one section are ordered from 1 to 10 to have a linear voltage distribution with equal voltages between two adjacent wires [13]. Except for the first (1) and the last layer (10), effects due to capacitive currents through the interturn capacitances are minimized. To reduce an error due to different winding resistances and stray inductances of the ten wires of the IVD, caused by the different wire lengths, the order of the layers is alternately reversed in adjacent sections. The second octad of the IVD (W8) is wound in two turns of eight twisted wires.

C. Ratio Sampling System

The scheme of the sampling-based voltage comparator "HRPM MKII" for measuring the complex voltage ratio $\underline{\Gamma}_{21} = \underline{U}_2 / \underline{U}_1$ is shown in Fig. 5. It contains analogue-to-digital converters (ADC, NI 9239) with a differential pre-stage, a 32-bit digital IO switching module (NI 9403), a 16-bit digital-to-analogue converter (DAC, NI 9263), some circuitry for choosing the synchronization source, a voltage source derived from the 50 Hz power supply and an active attenuator.

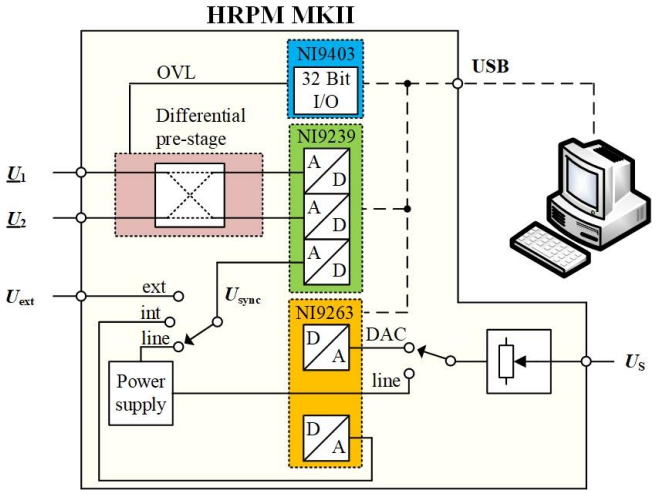

Fig. 5. Scheme of the sampling-based voltage comparator.

The section for capturing the voltage signals U_1 and U_2 and the synchronization signal U_{Sync} makes use of a 24-bit sigma-delta ADC with sampling rates of up to 50 kS/s and a differential pre-stage. To supress the inherent mismatch of the two signal channels, the inputs are alternately being interchanged. This ensures high accuracy for the measured complex voltage ratio $\underline{\Gamma}_{21}$ [14]. Due to the simultaneous sampling process of the ADC's channels, no substantial deterioration of the accuracy with power line signals occurs.

As the digitizer is operated in an asynchronous sampling process, a resampling algorithm which interpolates the sampled dataset was developed to avoid spectral leakage [15]. The typical accuracy obtained at power frequencies by means of the system presented here is, for complex voltage ratios $0 \le \underline{\Gamma}_{21} \le 1$, in the order of $5 \cdot 10^{-7}$ for the real and imaginary part. The pre-stage has been recently improved. It provides two voltage ranges of ± 10 V and ± 1 V to achieve a better signal-to-noise ratio for voltages below 1 V. Further improvements are related to the input buffers, the MOS switch, the instrumentation amplifiers with selectable gain and the low-pass filters. Compared to the first HRPM version, these measures lead to lowered uncertainties of the measured ratio.

III. Measurement Results

A. Active LV Capacitor

Figure 6 shows the simplified calibration circuit to validate the behaviour of the ALVC. For measuring the input current $\underline{I}_S$ and the output voltage $\underline{U}_2$ of the ALVC, a buffered resistor R_N = 10 kΩ with low phase errors and the here presented two-channel sampling system have been used.

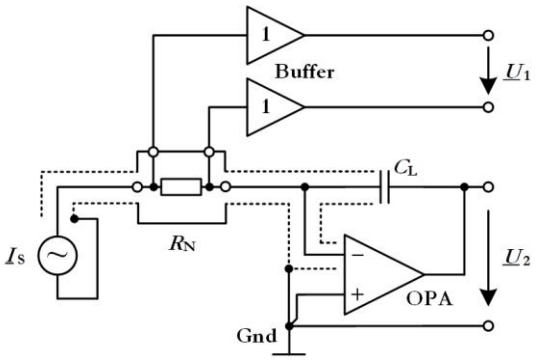

Fig. 6. Setup of the calibration scheme to calibrate the active LV capacitor.

From the measured complex ratio $\underline{\Gamma}_{21} = \underline{U}_2 / \underline{U}_1$, the impedance $\underline{Z}_C$ of C_L was calculated using $-R_N \cdot \underline{\Gamma}_{21}$. The phase displacement due to the small differential input capacitance from the two buffer inputs have been calibrated in-situ and numerically corrected in the calculation of $\underline{Z}_C$. From $\underline{Z}_C$ the capacitance C_L and the phase displacement δ to -90 ° is calculated from $C_L = (2 \cdot \pi \cdot f \cdot |\underline{Z}_C|)^{-1}$ and $\delta = \arg\{\underline{Z}_C\} + \pi / 2$. As the ALVC in conjunction with R_N follows an integrator function, a transconductance amplifier with isolation transformer was used as a current source. Compared to the use of a voltage source, it was found that the current source eliminates the low frequency noise with f^1 characteristics of the output voltage U_2 of the ALVC. The results for all individual capacitances C_{L1} to C_{L17} and their associated tan δ at 62.5 Hz

are shown in Table I. The deviation $\Delta C/C$ from its nominal value C_n of the majority of the capacitances C_{L1} to C_{L17} are within 0.1 %, whereas some of the 500 nF capacitors are within 1 %.

TABLE I
CALIBRATION RESULTS FOR ALL CAPACITORS AT 62.5 HZ

No	C_n in nF	$\Delta C/C$ in µF/F	$\Delta C/C(U)$ in µF/F	tan δ
1	500	-6360	0.4	12.4
2	500	-5589	-0.2	11.4
3	100	483	-0.1	11.1
4	200	268	0.2	10.9
5	100	693	-0.1	10.7
6	500	675	0.3	12.5
7	500	-514	0.4	12.3
8	500	-6150	0.3	12.2
9	500	764	0.3	12.5
10	500	110	0.3	12.7
11	500	-2851	0.2	13.1
12	500	-10	0.3	13.2
13	500	-3619	0.3	13.4
14	500	765	0.4	12.8
15	500	614	0.3	12.9
16	500	752	0.2	13.3
17	500	771	0.2	14.0

The tan δ for each capacitor is around 11 ppm for the 100 nF and 200nF capacitors and vary from 12.2 ppm to 14 ppm for the 500 nF capacitors. It seems to be that the tan δ for capacitors around the sense point at C_{L8} is minimal, meaning that a small series resistance of the relevant PCB track contributes to a slightly increased tan δ for the outer capacitors. The values for $\Delta C/C(U)$ show the measured relative differences of each capacitor at 100 % (e.g. 6 V) and 10 % (0.6 V) to get an indication of their voltage dependence.

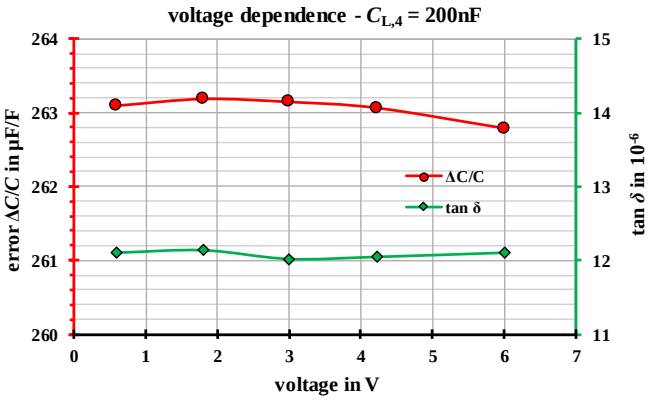

Fig. 7. Voltage dependence of the 200nF capacitor at 79 Hz within a voltage range up to 6 V.

A more detailed view to the attained voltage dependence is shown in Fig. 7 for C_{L4} = 200nF. Here the frequency was adjusted to 79 Hz, as in this case the impedance of C_L is around 10 kΩ for which the measured voltage ratio U_2 / U_1 is around one, with best possible uncertainty in the order 0.2 ppm (k = 2). Between 0.6 V to 6 V a change of the capacitor within ± 0.2 µF/F can be observed. The trend is slightly quadratic, whose origin might be a self-heating of the reference resistor R_N as well. For the tan δ no visible change within ± $0.1 \cdot 10^{-6}$ can be observed. For the voltage dependence, a standard uncertainty $u(\Delta C/C(U))$ = 0.2 µF/F and $u(\tan \delta(U)) = 0.1 \cdot 10^{-6}$ will be used for all capacitors C_{L1} to C_{L17}.

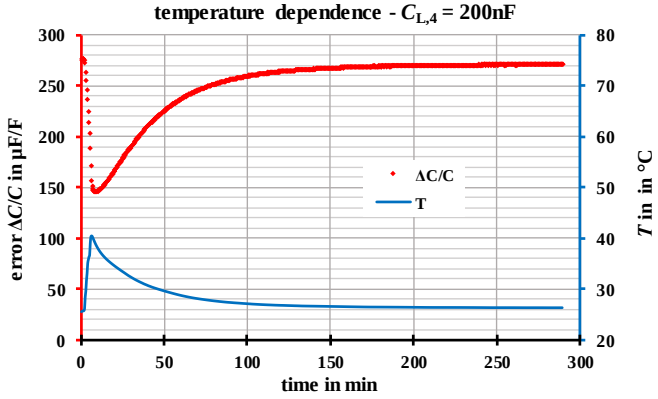

Fig. 8. Temperature characteristics of the 200nF capacitor between 23 °C and 40 °C at 62.5 Hz and 6 V.

To obtain the temperature characteristics of C_L, the temperature inside the case of the ALVC was increased with a hot air gun and measured via a PT 1000 sensor. The change of the capacitor C_{L4} with temperature over the time is shown in Fig. 8. The first 5 minutes the temperature increases from 26 °C to 40 °C, while the capacitor changes by around 120 µF/F. After that time the heat source is switched off and the casing is closed. The following 200 minutes the temperature settles back to 26 °C, while the capacitor changes simultaneously to its initial value at t = 0. A hysteretic effect cannot be seen. From that measurement, a temperature coefficient (TC) of around 10^{-5} / K is found. It is believed that the other capacitors of the ALVC behave similarly. The change of the tan δ for the temperature change of 14 K was only 0.5 ppm (TC around 0.03 ppm/ K) and can therefore be neglected.

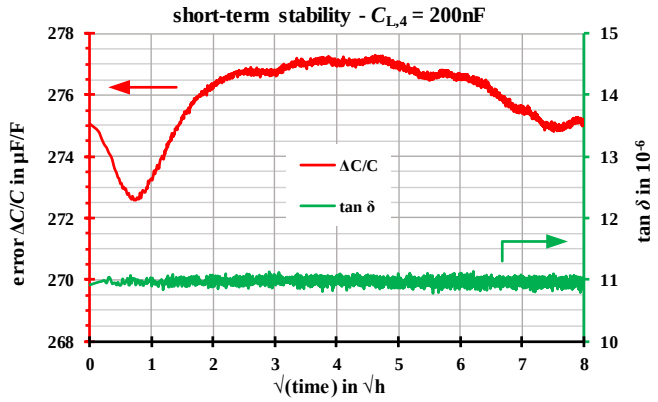

Fig. 9. Short-term stability of the 200nF capacitor at 62.5 Hz and 6 V. To have a better time resolution at the beginning of the measurement, the square-root of the time has been chosen for scaling the x-axis.

Finally, the short-term stability of the capacitor C_{L4} has been measured over a time of 64 h. The result for C_{L4} and its tan δ is

shown in Fig. 9. Note the non-linear scaling of the x-axis with √t. It can be seen, that the stability of C_L is in the range of ± 2.5 µF/F and ± 0.1 ppm for its tan δ. This variation of C_L is possibly due to the regulation of the air condition in the shielded room, which is in range of 0.5 °C for the temperature. The higher drift of the capacitor in the beginning (-2.5 ppm / h) is due to the setting of the capacitor with opened case, where a sudden change of the device-internal temperature occurs. However, when using the ALVC with the high voltage capacitor as a CVD in the step-up measurements according to (1), temperature changes in the order of 0.5 °C within 30 min in the HV laboratory can be expected. With the TCs of around 10^{-5} / K for the ALVC and the HV capacitor as well, the CVD ratio can easily change within 5 ppm. Therefore, a numerical compensation for this ratio change is required. The easiest way is to repeat the transfer measurements according to (1) in the reversed order (step (I) → step (II) → step (I)) and in an equidistant time interval, e.g. in 15 min. By taking the average of the two measurements in this three-point transfer cycle, a first order drift of the CVD is compensated. In this case a remaining standard uncertainty contribution of 10 % of the expected drift of 5 ppm for the CVD ratio of $u(\underline{F}_{CVD}) = 0.25$ ppm and 0.1 µrad can be reasonably assumed.

B. *Hybrid Voltage Transformer for Scaling*

The realized hybrid voltage transformer VT_H (see section II.B) allows to calibrate separately the ratio error of the first VT section and the ratio error of the second IVD section. The VT section with a fixed ratio of $K_n = 10$, was calibrated with an IVD at power frequencies. The result for the ratio error ε_{VT} at 62.5 Hz is -0.7 ppm, while the phase error is $\delta_{VT} = -0.6$ µrad. The associated standard uncertainty is $u(\varepsilon_{VT}) = u(\delta_{VT}) = \pm 0.15$ ppm (or µrad). The error change with varying primary voltages between 10 V and 100 V is within 0.1 ppm.

The IVD section was calibrated by using a build-up method [16], whereas the two auxiliary windings W5 and W6 have been used as reference windings. The separate screen of W5 and W6, driven by an external IVD, ensures a small common mode error of the reference winding, during the build-up process. This common mode error has been found to be in the order of $5 \cdot 10^{-9}$ (quadrature) when driving the screen with the full input voltage of the IVD. The common mode error is cancelled out in the build-up process of the IVD, as both windings, the secondary which is the IVD input, as well as the reference winding in use are affected simultaneously due to the magnetic coupling of these windings with core C2 (see Fig. 4).

Figure 10 shows the results for the in-phase and quadrature corrections α_{IVD} and β_{IVD} of the first decade of the IVD at a primary voltage of 100 V (10 V IVD input) and 62.5 Hz. The corrections are well within ± 15 nV/V (RTI), meaning that the ratio errors of the IVD (RTO) are well within 0.05 ppm and 0.1 µrad for any setting of the taps from 0.1 to 1.0. The corrections for the tap 0.0 has been found to be within $2 \cdot 10^{-9}$. At an excitation of 10 % (i.e. at 1 V IVD input), the corrections deviate by no more than $2 \cdot 10^{-9}$, so that the IVD section might be considered as independent from the primary input voltage of VT_H. The results for the second octad of the IVD (not shown here) are one magnitude of error smaller, i.e. below $1 \cdot 10^{-9}$, meaning that the second octad does not significantly contribute to the IVD corrections. A very recent development is the measurement system for the IVD build-up calibration. Although it is not yet fully characterized, a conservatively estimated standard uncertainty of $5 \cdot 10^{-9}$ can be assumed.

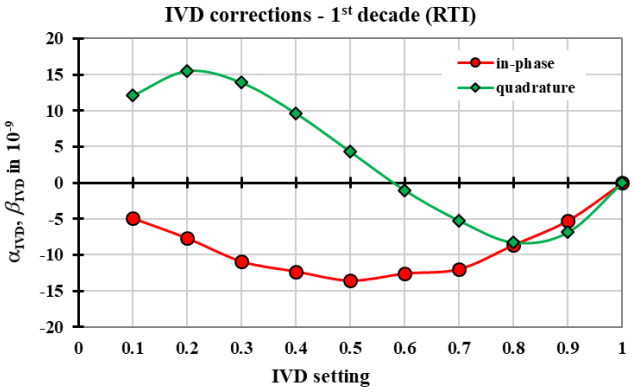

Fig. 10. In-phase and quadrature correction referred to the divider input voltage (RTI) of the first decade of the IVD section of VT_H.

Especially for the intended use of VT_H in the two steps of the presented step-up method according to (1), only the ratio error difference of VT_H for the two setting $D_H(I)$ and $D_H(II)$ is important. As the error of the VT section is cancelled out in the expression $\underline{F}_H(I) / \underline{F}_H(II)$ in (1), only the difference of the IVD correction $\alpha_{IVD}(I) - \alpha_{IVD}(II)$ and $\beta_{IVD}(I) - \beta_{IVD}(II)$ in the two settings I and II remains. As a fictive worst case in a step-up procedure, the two settings $D_H(I) = 0.05$ and $D_H(I) = 0.01$ for VT_H are assumed. The error difference of the IVD is about 10^{-8} for $\alpha_{IVD}(I) - \alpha_{IVD}(II)$ as well as for $\beta_{IVD}(I) - \beta_{IVD}(II)$. The ratio error difference (RTO) would be 0.02 ppm and 0.11 µrad. To have a conservative uncertainty contribution in the uncertainty budget, an uncorrelated standard uncertainty $u(\underline{F}_H(I)) = u(\underline{F}_H(II)) = 0.1$ ppm and 0.15 µrad have been take into account.

C. *Ratio Sampling System*

For evaluating the performance of the sampling-based voltage comparator (HRPM), the attainable ratio and phase accuracy of $\underline{\Gamma}_{21} = \underline{U}_2 / \underline{U}_1$ have to be verified.

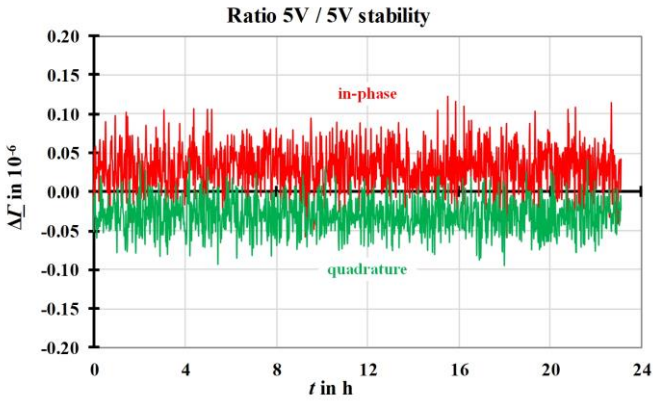

Fig. 11. Stability of the ratio and phase error at a voltage ratio 5V / 5V.

Figure 11 shows the error and the stability of this complex ratio for equal input voltages of 5 V and at 62.5 Hz, measured over almost 24 h. The sampling time has been adjusted to 2 s, while 30 readings were used for the averaging. The averages of the in-phase and quadrature error are well below 0.1 µV / V with a scattering of around ± 0.07 ppm. No drift is discerned. The ratio and phase accuracy at varying ratios from $0 \le \underline{\Gamma}_{21} \le 1$ has been determined using the IVD section of VT_H (see Fig. 10). The primary voltage was set to 50 V, so that the IVD input voltage of 5 V, and the IVD output has been used as input voltages $\underline{U}_1$ and $\underline{U}_2$ of the HRPM. Figure 12 shows the error of the measured complex ratio from 0 V / 5 V to 5 V / 5V. It is clearly visible for ratios around zero and around one, that the in-phase component $\mathrm{Re}\{\Delta\underline{\Gamma}_{21}\}$ of the error is well within 0.2 µV / V. At ratios between 0.3 to 0.7 the highest deviation of 0.4 µV / V occur. This is probably due to small nonlinearities of the used ADC channels, that cannot be automatically cancelled by the ADCs pre-stage within the HRPM.

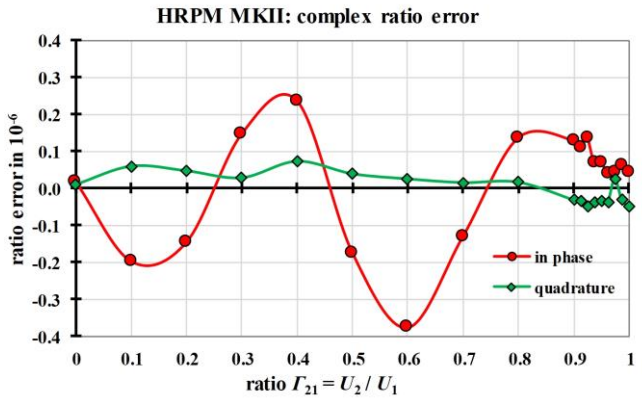

Fig. 12. Deviation of the measured ratio and phase of the Ratio Sampling System versus an IVD.

A similar ratio-dependency for the deviations of the quadrature component $\mathrm{Im}\{\Delta\underline{\Gamma}_{21}\}$ cannot be observed. These results agree well within 0.1 µV / V. The most likely voltage ratios are in the range of 0.9 to 1.1, as the hybrid voltage transformer is adjusted within its resolution in the two steps of the proposed step-up method according to (1), for getting almost equal voltages U_1 and U_2. Therefore a contribution for the (relative) standard uncertainty $u_r(\underline{\Gamma}_{21})$ for the ratio and the phase of the complex ratio is 0.1 ppm (or µrad). In case of using the system at a ratio of 1:2 or 2:1 (for example, 3V / 6 V) a standard uncertainty of ± 0.5 ppm and 0.1 µrad would better describe the accuracy of the HRPM.

IV. Attainable Uncertainty for the Step-Up Method

The model equation for the step-up measurement using the CVD as a transfer element is given in (1). With additional uncertainty contributions for the voltage dependence of the ALVC, of the high voltage capacitor, and for the short-term stability of the CVD, the details of the uncertainty calculations Type B for the transformer voltage error $u(\varepsilon)$ and its phase displacement $u(\delta)$ are given in Table II. To achieve the small uncertainty for the voltage dependence $u(\Delta C_H)$ it is assumed that the HV capacitor(s) from PTB with the smallest voltage dependence of around 1 ppm, and for an excitation of maximum 50 % of its rated voltage has been chosen. The small contribution for the short-term stability $u(\underline{F}_{CVD})$ has been obtained using the described three-point transfer cycle (see section III.A).

TABLE II
Uncertainty Budget (Type B only) for the Step-Up Method for Standard Voltage Transformers

quantity		ratio error $u(\varepsilon)$	phase error $u(\delta)$
ratio measurement I	$\underline{\Gamma}_{21}$ (I)	0.10 µV/V	0.10 µrad
ratio measurement II	$\underline{\Gamma}_{21}$ (II)	0.10 µV/V	0.10 µrad
divider ratio setting I	$\underline{F}_H$(I)	0.10 µV/V	0.15 µrad
divider ratio setting II	$\underline{F}_H$(II)	0.10 µV/V	0.15 µrad
voltage dependence C_{HV}	ΔC_H	0.20 µF/F	0.10 µrad
voltage dependence C_{LV}	ΔC_L	0.20 µF/F	0.10 µrad
short term stability CVD	F_{CVD}	0.25 µV/V	0.10 µrad
result transfer I to II	ε_Γ, δ_Γ	**0.43 µV/V**	**0.31 µrad**
standard VT(n-1)	ε_N, δ_N	2.0 µV/V	2.0 µrad
result VT(n)	ε_X, δ_X	**2.05 µV/V**	**2.02 µrad**

A typical standard deviation in the measurement is below 0.2 ppm (or µrad), so that the Type A uncertainty is well below 0.1 ppm (or µrad). The given combined standard uncertainty in Table II would therefore not substantially increase. The first results $u(\varepsilon_\Gamma)$ and $u(\delta_\Gamma)$ are the standard uncertainties for the transfer without considering the contribution of VT(n-1). These are around 0.9 ppm and 0.7 µrad for $k = 2$ and represents the loss of accuracy due to the presented step-up method. When considering typical attainable standard uncertainties of 2 ppm and 2 µrad of the previously calibrated VT, acting here as the reference VT(n-1), it can be seen that the resulting calibration results $u(\varepsilon_X)$ and $u(\delta_X)$ for the transformer under test VT(n) will only slightly be degraded by the transfer itself.

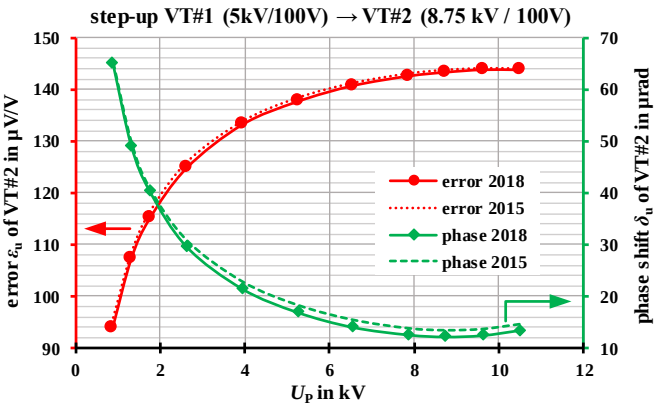

Fig. 13. Results of the ratio error (circles) and phase error (diamonds) of the presented step-up method (2018) and compared to the results (dashed and dotted curves) of another CVD-based step-up method (measured in 2015) for the standard VT #2 with the ratio 8.75 kV / 100 V.

A very simplified estimation for the six standard VTs from 5 kV to 800 kV / √3 show that for the highest rated VT a standard uncertainty in the order of $\sqrt{6} \cdot 2\ \text{ppm} \approx 5\ \text{ppm}$ is achievable. The results for a VT calibration with the presented build-up method has been compared to the results achieved with another more complex CVD-based build-up method developed around 2012. Due to its complexity, this elder build-up method has not been published. The transfer has been done from the ratio 5 kV / 100 V (VT #1) to the ratio 8.75 kV / 100 V (VT #2). Figure 13 shows the results for an excitation of 10 % to 120 % of the rated primary voltage of VT #2. Although this VT exhibits a large error span, the agreement between both methods is within 1 ppm and 2 µrad. This gives a clear evidence that the presented new step-up method is properly working.

V. Conclusion

A new fundamental step-up method for standard voltage transformers has been presented, and the setup of the required components has been discussed. The main component is an active low-voltage capacitor, designed to realize various capacitive voltage divider ratios by means of compressed–gas, high-voltage capacitors for rated primary voltages between 5 kV and 800 kV / √3. It has been verified, that this divider has a negligible voltage dependency and low phase errors around 50 / 60 Hz. The other components, mainly a two-stage voltage transformer with integrated inductive voltage divider and a sampling-based voltage comparator allow to achieve a transfer uncertainty for one build-up step of below $1 \cdot 10^{-6}$ ($k = 2$).

References

[1] G. Ramm, and H. Moser: “Eine neuartige, rechnergesteuerte und selbstkalibrierende Spannungswandler-Meßeinrichtung”, PTB-Mitteilungen, Vol. 106, 4/96

[2] H. Schering, "Brücke für Verlustmessungen," Zeitung für Instrumentenkunde, Tätigkeitsbericht der PTR, vol. 40, pp. 124, 1920

[3] N. L. Kusters and W. J. M. Moore, "The Compensated Current Comparator; A New Reference Standard for Current-Transformer Calibrations in Industry," IEEE Trans. Instrum. Meas., vol. IM-13, no. 2 & 3, pp. 107-114, June-September 1964

[4] A. Braun and H. Richter: “Determination of Voltage Transformer Errors by Means of a Parallel-Series Step-Up Method,” IEEE Trans. Instrum. Meas., vol. 29, No. 4, pp. 490-492, Dec. 1980.

[5] H. G. Latzel and K. Schon: “Precise capacitance measurements of high-voltage compressed gas capacitors,” IEEE Trans. Instrum. Meas., vol. 36, No. 2, pp. 381-384, June 1987.

[6] O. Petersons and S. P. Mehta: “An active high-voltage divider and phase shifter,” IEEE Trans. Instrum. Meas., vol. 36, No. 2, pp. 362-368, June 1987.

[7] E. Mohns, J. Chunyang, H. Badura and P. Raether: “An Active Low-Voltage Capacitor for Capacitive HV Dividers,” CPEM 2018 Conference Digest.

[8] E. Mohns, G. Roeissle, S. Fricke and Florian Pauling: “A Sampling-Based Ratio Bridge for calibrating Voltage Transformers,” CPEM 2018 Conference Digest.

[9] Wikipedia https://en.wikipedia.org/wiki/Ceramic_capacitor.

[10] S. Awan, B. Kibble and J. Schurr: *Coaxial Electrical Circuits for Interference-Free Measurements*, IET electrical measurement series 13, 2011.

[11] W. G. Kürten Ihlenfeld and R. T. B. Vasconcellos: “On the Nonlinear Voltage Dependence of Passive Electronic Components,” CPEM, Rio de Janeiro, 2014.

[12] OMEM, “TA42”, see www.omemspa.com.

[13] G. W. Small, I. Budowsky, A. M. Gibbes, and J.R. Fiander: “Precision Three-Stage 1000 V/50 Hz Inductive Voltage Divider,” IEEE Trans. Instrum. Meas, Vol. 54, No. 2, pp. 600-603, April 2005.

[14] E. Mohns, G. Roeissle, S. Fricke and F. Pauling: "An AC Current Transformer Standard Measuring System for Power Frequencies," IEEE Trans. Instrum. Meas.,vol. 66, no. 6, pp. 1433-1440, June 2017, DOI: 10.1109/TIM.2017.2648918.

[15] E. Mohns, S. Fricke, C. Jäschke, and P. Schegner: “A Current Clamp based High Voltage Monitoring System,” AMPS 2015 Conf. Digest, Aachen, September 2015.

[16] A. M Thompson, “Precise calibration of ratio transformers,” IEEE Trans. Instrum. Meas, Vol. IM-32, pp. 47-50, March 1983.

Enrico Mohns was born in Bautzen, Germany, in 1973. He received his Dipl.-Ing. (FH) degree from the Braunschweig-Wolfenbüttel University of Applied Sciences in 2001, and his Dipl.-Ing. (TU) and Ph.D. degrees from the Technical University Braunschweig, Germany, in 2007 and 2013, respectively. In 2001, he joined the Physikalisch-Technische Bundesanstalt, Braunschweig, where he has been engaged in the field of electric power measurement techniques. Since 2008, he has been head of the Working Group “Instrument Transformers and Sensors”.

Chunyang Jiang was born in Qiqihaer, China, in 1985. He received a B.S. degree in Electrical Engineering and Automation from the Dalian University of Technology, Dalian, in 2008, and an M.S. degree in High-Voltage Insulation Technology from the Huazhong University of Science and Technology, Wuhan, in 2011. From 2011 to 2012, he was an engineer assistant with the State Grid Electric Power Research Institute. In 2012, he joined the China Electric Power Research Institute. His research interests include high-voltage insulation and high-voltage and heavy current measurement technology.

Henrik Badura was born in Groß Strehlitz, Poland, in 1974. He received his B.Eng. degree in electrical engineering in 2015. In 2015, he joined the Physikalisch-Technische Bundesanstalt in Braunschweig, where he has been active in the Working Group “Instrument Transformers and Sensors”.

Peter Räther was born in Berlin, Germany, in 1966. He received his Dipl.-Ing. (FH) degree in 1996. In 1997, he joined the Physikalisch-Technische Bundesanstalt. Since 1999, he has been engaged in the field of electric power measurement techniques.