

Economic high resolution fringe counting for heterodyne interferometers using FPGA technology

Felix Meli*

Federal Institute of Metrology METAS, Lindenweg 50, CH-3003 Bern-Wabern, Switzerland

* Corresponding author: felix.meli@metas.ch

Abstract

Simple FPGA PCI boards are capable of capturing digital signals up to 40 MHz and analogue signals up to 200 kHz, making them suitable to replace whole machine controllers of multi-axis measuring machines. Unfortunately capturing a 4 MHz heterodyne signal (beat frequency) at a 40 MHz rate will result in a poor phase interpolation. We present a statistical approach to the phase evaluation while maintaining a reasonably high data rate and synchronicity with acquired analogue signals. Sub-nanometre resolution is achieved by averaging counter values sampled asynchronously to the beat frequency. The implemented FPGA program allows signal processing for three simultaneously captured interferometer positions with synchronized 8 channels A/D in- and output, interpolated A-B encoder output signals (usable for motion controller boards) and high speed DMA data transfer to the PC memory all on one PCIe board. Fringe counting works up to 6 MHz covering a speed range of more than ± 0.4 m/s. The implemented 64 bit position counters cover measurements up to several meters with sub nm resolution.

1 Introduction

Interferometry is a fundamental method for traceable dimensional measurements. Homodyne and heterodyne detection is equally used for fringe counting and interpolation. While the heterodyne technology is less sensitive to intensity variation, high resolution fringe detection is more demanding. With beat frequencies in the order of a few MHz, phase-locked-loops (PLLs) and counters operating at several hundred MHz are required to achieve sub nanometre resolution. Besides interferometer data, measurement processes often need various other analogue sensor signals to be captured synchronously with position (fig. 1).

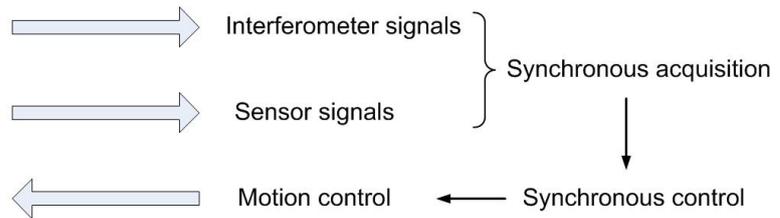


Figure 1: Data acquisition and control requirements for typical metrology systems consist of multiple axis heterodyne interferometer, analogue sensor signals and control output signals

With the ongoing changes of PC operating systems and hardware, it becomes necessary to rebuild complex PC based machine controllers several times during machine life with relatively high personal efforts and costs especially for multi axis systems. For the retrofits of the METAS photomask measuring machine [1] and the METAS μ -CMM [2] we therefore studied the application of FPGA boards containing analogue and digital in- and outputs which can be easily programmed in

the high level language LabView. Such FPGA boards are capable of capturing digital signals up to 40 MHz which, using the classical counting approach will result in a poor phase interpolation in the order of 16 nm. However, because of the relatively low characteristic frequencies of mechanical systems, position data at MHz rate is not required. The here presented statistical approach to the phase evaluation provides high resolution at still reasonable data rate and synchronicity with acquired analogue signals.

2 Heterodyne interferometry

The classical approach to the phase interpolation for heterodyne interferometers is by using a PLL. The reference and heterodyne frequency $f_{\text{het}} = f_1 - f_2$ are multiplied by an interpolation factor and then counted. For sub nanometre resolution of single pass interferometers this interpolation factor is > 300 . In a heterodyne interferometer the frequency of the measurement signal shifts with the velocity of the target mirror. A heterodyne frequency of 3 MHz allows for target speeds of almost 1 m/s (single pass) leading to a frequency range of the measurement signal of 0 – 6 MHz (fig. 2). The classical approach requires therefore PLLs and counters which can operate in the GHz range.

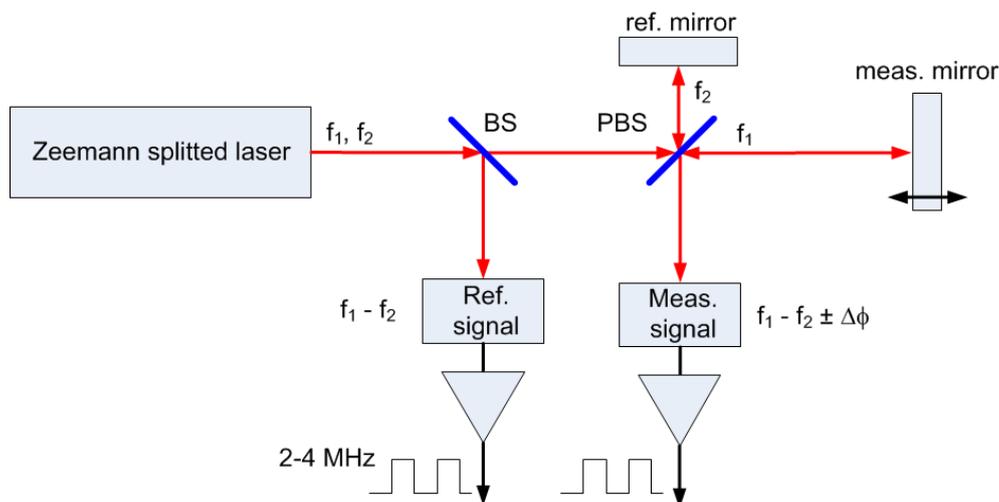


Figure 2: Principals of a heterodyne interferometer.

Phase measurements and fringe counting using FPGA were already proposed by others [3, 4]. In these cases the phase measurement and the counting is done in separate steps. The phase measurement is done by direct analogue to digital conversion of the reference and the measurement signals. The FPGA calculates then the phase shift between the two digitised sinusoidal waveforms. This result is combined with the fringe counter to provide the interpolated position over longer distances. The maximum target speed is limited by the AD conversion rate. Using very sophisticated AD-converters and very fast FPGAs the rate can be as high as 100 MHz [3].

The approach presented here does not require AD converters nor PLLs and works with conventional (40 MHz) FPGA circuits. The phase measurement and the counting are done in a single step giving directly the interpolated position. In order to be compatible with the already existing interferometer and preamplifier hardware (Agilent), the reference and the measurement signals at the input are not sinusoidal anymore but rectangular binary waves (fig. 2).

3 Principals and implementation

3.1 Statistical approach to phase evaluation

In the following we present a statistical approach to the phase evaluation with potentially high resolution while maintaining a reasonably high data rate and synchronicity with simultaneously acquired analogue signals.

Capturing a 4 MHz heterodyne signal (beat frequency) at a 40 MHz rate will, using a simple counting approach, result in a poor phase interpolation. For a 633 nm HeNe laser and a double path interferometer the such obtained resolution is about 16 nm. Because of the relatively low characteristic frequencies of mechanical systems, position data is usually not required at a MHz rate and considerable averaging can be used. Here, the resolution is enhanced by averaging counter values sampled asynchronously to the beat frequency. The resolution is variable and increases with decreasing bandwidth (increasing averaging period). Averaging is performed on the FPGA board and allows bandwidths between 160 kHz and 2.4 Hz with several steps in between. The same averaging process is simultaneously applied to the analogue input signals and therefore data synchronicity is maintained even at bandwidths below 160 kHz.

The implemented FPGA program allows signal processing for three simultaneously captured interferometer positions with synchronized 8 channels A/D in- and output, interpolated quadrature signal outputs, usable for motion controller boards, and high speed DMA data transfer to the PC memory all realised on a single PCIe board. Fringe counting works up to 6 MHz covering a speed range of roughly ± 0.5 m/s (double path). 64 bit counter registers are used to cover measurements up to several meters with sub nanometre resolution.

In addition, loss of lock, induced when moving too fast, and signal loss, when the interferometer beam is interrupted, are detected. Figure 3 shows a block diagram of the heterodyne interferometer controller implemented on a Multifunction-RIO board with a Virtex-5 LX30 FPGA from National Instruments.

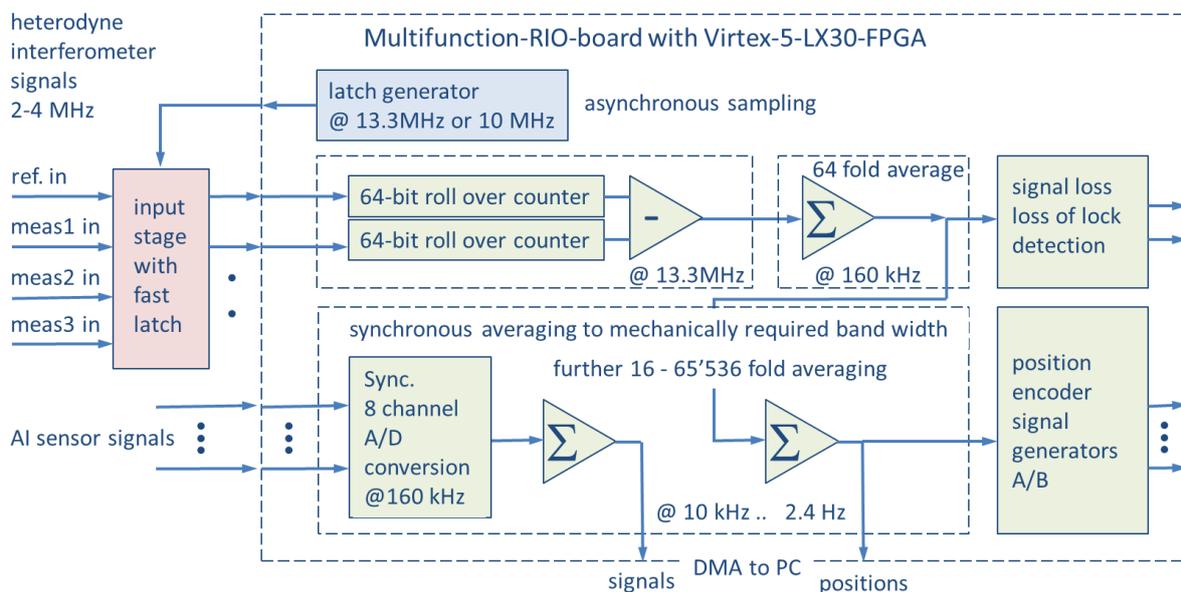


Figure 3: Block diagram showing the asynchronous sampling and averaging performed on the FPGA PCIe board.

3.2 Preamplifier and latch

A crucial element is the preamplifier with latch. It is a very simple additional electronic circuit between the optical signal preamplifier (here an Agilent 10780F remote receiver) and the FPGA board. It is needed to adjust the digital signal level of the receiver output and the FPGA digital inputs. It consists of a line receiver with matched input impedance in order to avoid signal reflections. The output of the line receiver goes to a fast signal latch. The latch trigger is generated by the FPGA board and it freezes all input states within a few picoseconds. The exactly simultaneous capturing of the reference and measurement signals from the interferometer is important for the accuracy of the following statistical evaluation.

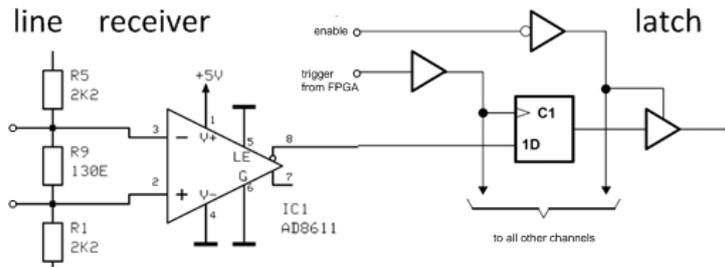


Figure 4: Input signal conditioning and fast signal latch.

4 Experimental

4.1 Synthetic signal fringe counting properties

First synthetic interferometer signals were used to determine the properties of the implemented FPGA phase measurement. Using synthetic input signals, generated by two function generators (Stanford Research Instruments, DS 345, fig. 5), the resolution limits and the phase linearity were tested. The heterodyne frequency used for the simulation (2.710 Mhz) was the same as the Zeemann frequency splitting of the real laser used later on in the practical test (Agilent 5519A Laser Head). The phase shifting properties of the two function generators was assumed to be ideal.

The RMS position noise measured was 6 pm at 20 Hz and 500 pm at 10 kHz (fig. 6). The electronic phase interpolation non-linearity was ± 170 pm measured at 20 Hz bandwidth. The FPGA latch trigger rate was 13.3 Mhz (fig. 7). The remaining non-linearity is probably caused by signal reflections in the cabling. Impedance matching becomes crucial in order to avoid any signal flank deformations. Sharp and stable signal flank shapes are necessary to define a meaningful phase shift between two digital signals. Some influence of the function generators can not be excluded.

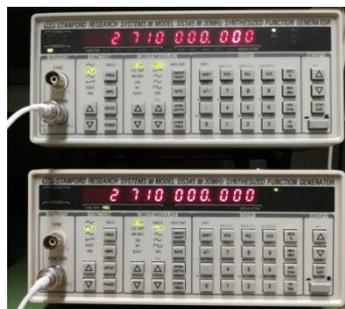


Figure 5: Measured position noise (RMS) using reference and measure signals from two function generators. The simulated heterodyne frequency was 2.710 Mhz.

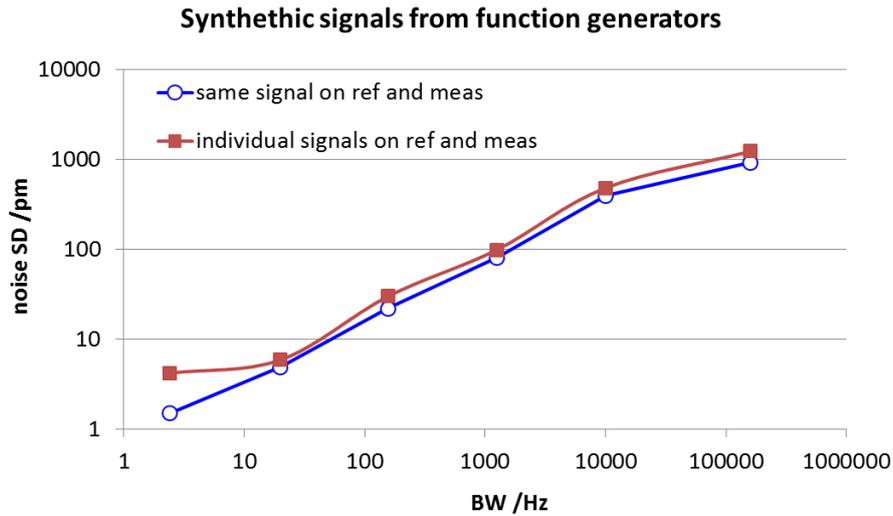


Figure 6: Measured position noise (RMS) using reference and measure signals from one or two function generators. The simulated Zeemann frequency was 2.710 Mhz.

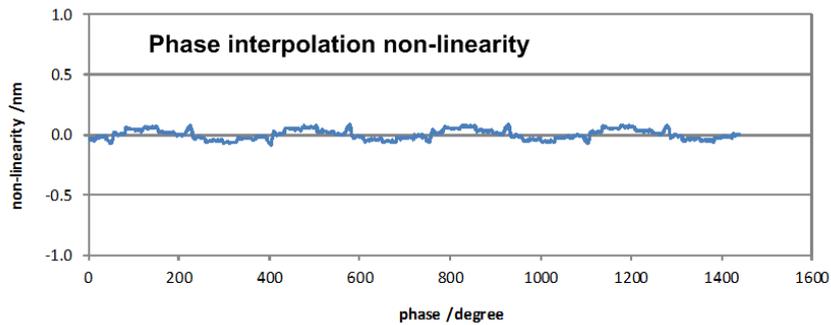


Figure 7: Measured position deviation vs. synthetic displacement created using signals from two function generators and phase shifts. Zeemann frequency: 2.710 Mhz, FPGA BW 20 Hz.

4.2 Experimental interferometer properties

The practical tests were performed using a Zeemann splitted HeNe laser (Agilent 5519A), a differential plane mirror interferometer (Agilent 10719A) and a remote receiver (Agilent 10780F). Small movements were produced with a piezo-actuated lever system having a reduction factor of 20.

The RMS position noise was 110 pm at 20 Hz and 400 pm at 10 kHz band width using a very short optical path of 5 mm (fig. 8). Increasing the optical path to 300 mm the RMS noise reaches a level of 1.6 nm (BW 156 Hz), essentially caused by air turbulence (fig. 9). This also shows the limits of a practical situation having interferometer beams in air. Here, a very high phase resolution of the electronics gives only little benefits.

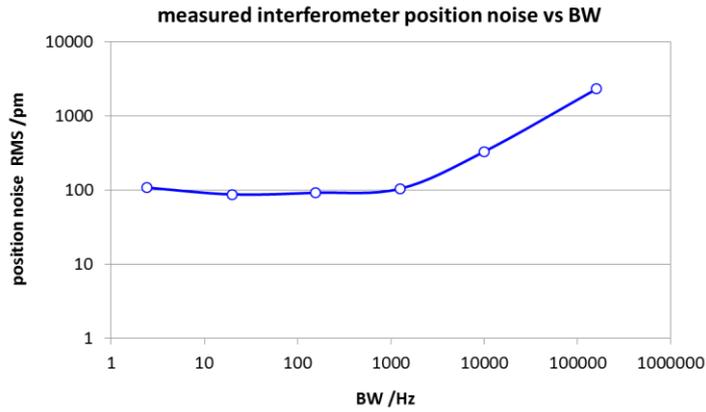


Figure 8: Measured RMS noise vs. BW. Single mirror target using a short optical path of 5 mm.

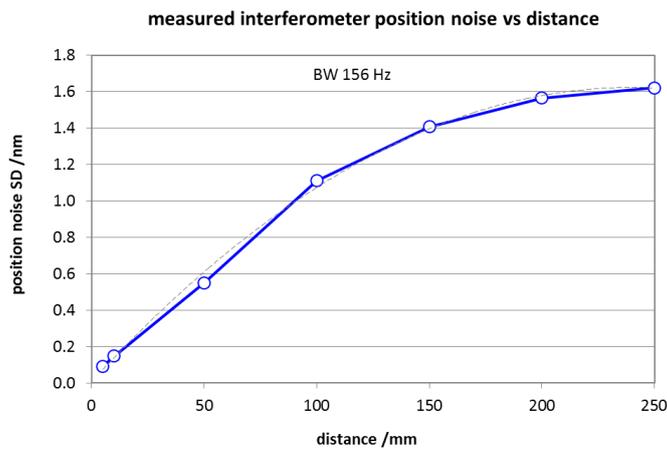


Figure 9: Measured RMS noise vs. distance. Single mirror target. BW 156 Hz. Noise caused by air turbulence (no beam protection).

Furthermore, many practical interferometers suffer from nonlinearities caused by phase mixing in the optics. Figure 10 shows a measurement of the non-linearity in the present interferometer setup. The non-linearity was measured to be ± 0.6 nm.

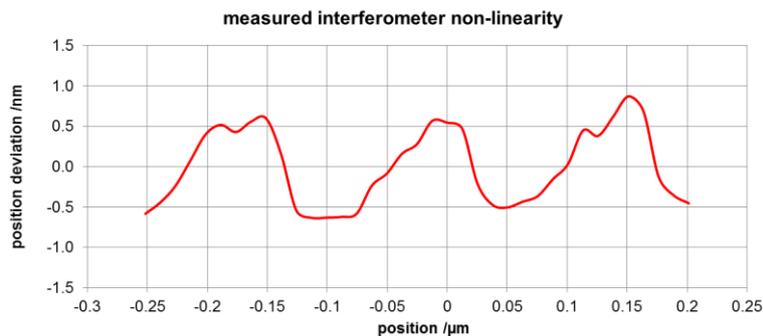


Figure 10: Measured non-linearity of the interferometer optics: ± 0.6 nm.

For illustration purposes the piezo lever system was set to perform 10 times 2 nm steps up and down. The interferometer measured the movement using a sampling rate of 156 Hz, noise and resolution allow to see clearly the 2 nm steps (Fig.11).

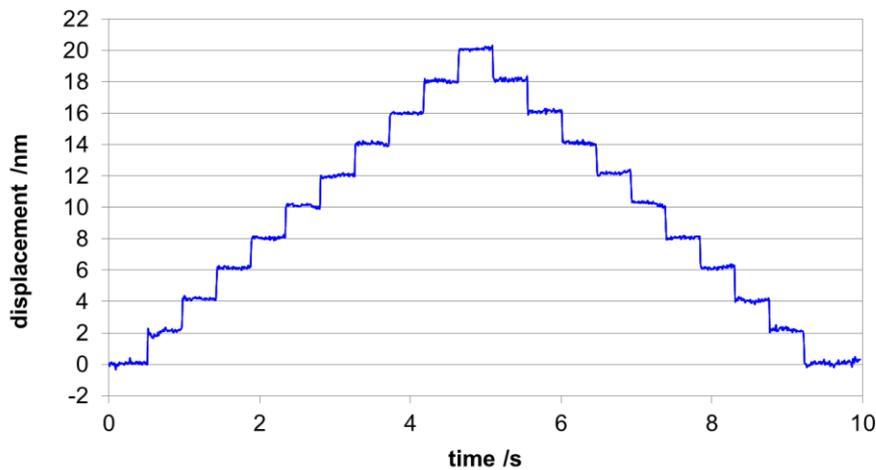


Figure 11: Piezo driven displacements measured with Agilent differential plane mirror interferometer and FPGA signal evaluation board. Data acquisition at 100 samples/s.

5 Numerical model and simulation of the interferometer resolution

Besides its simplicity the statistical approach to phase interpolation has also a clear disadvantage. The achievable resolution is not constant and depends in a complex way on the heterodyne beat frequency or more precisely on the ratio between the beat and the FPGA sampling frequency. The sampling frequency should not be a multiple of the heterodyne beat frequency because then the asynchronous averaging does not work anymore. But not only a simple multiple reduces the resolution, also any other rational relationship. An accurate simulation of the resolution should furthermore reproduce the two step averaging implemented in the FPGA which first averages 64 samples taken at 13.33 MHz and then continues to average these averages, synchronously with the analogue signal readings taken at a rate of 160 kHz, until the desired bandwidth limit is reached. Such a simulation was built into the high level program which communicates with the FPGA board. The FPGA measures the frequency of the reference signal and the simulation calculates a resolution map for a certain target speed range and all phase relations from 0 to 360°. Figure 12 shows such a map for a bandwidth of 1.25 kHz. In most cases a resolution below 0.2 nm can be reached.

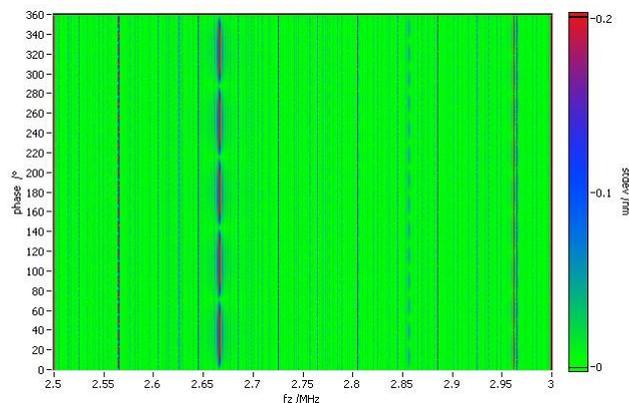


Figure 12: Simulated resolution (RMS) for beat frequencies from 2.5 MHz to 3.0 MHz and 0° to 360° phase for 1.25 kHz BW and 13.3 MHz sampling.

Using acousto optic modulators (AOMs) the heterodyne beat frequency can be chosen to achieve a good resolution. For a Zeemann splitted HeNe laser the beat frequency is fixed. If in such a case it happens that the resolution is not acceptable the FPGA sampling can be switched from 13.33 MHz to 10 MHz. This is illustrated in figure 13 for the highest bandwidth of 160 kHz.

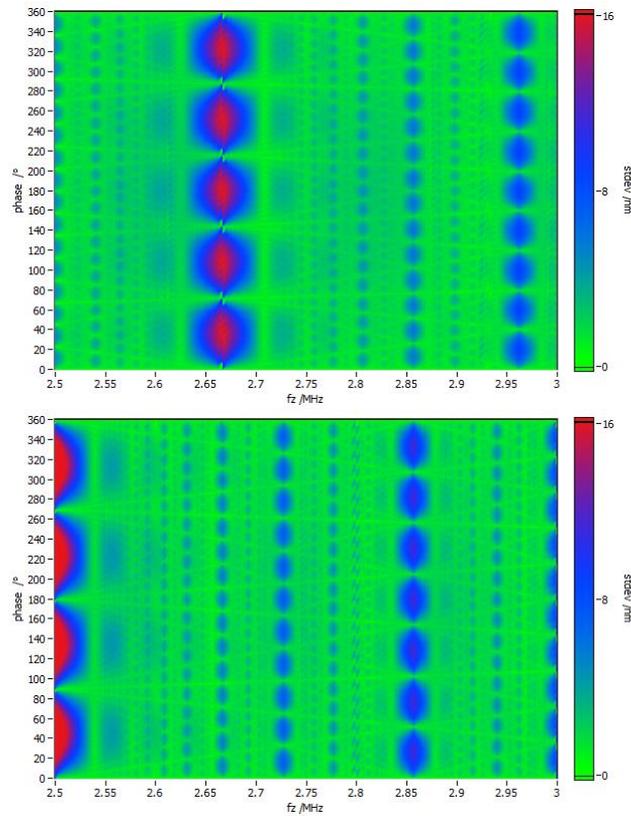


Figure 13: Simulated resolution (RMS) for Zeemann frequencies from 2.5 MHz to 3.0 MHz and 0° to 360° phase. For 160 kHz BW and 13.3 MHz sampling (top) and 10 MHz sampling (bottom).

In order to verify the simulation performance the resolution was measured using the synthetic signals from the two function generators. At a constant phase relation the frequency was swept from 2.5 MHz to 3 MHz. The measured resolution at 10 kHz bandwidth is compared to the simulation in figure 14. The black line (resolution) and the RMS value (red) are almost identical despite the complex structure.

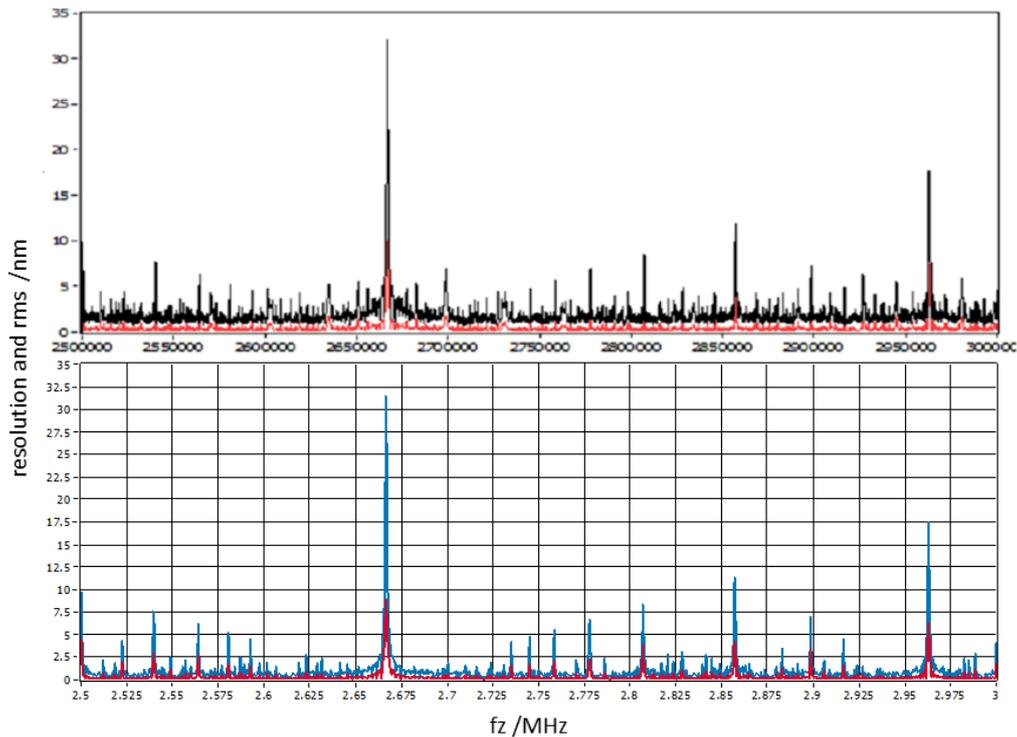


Figure 14: Synthetic signal measurement (top) and simulated resolution and rms (bottom) for $f_{het} = 2.5 - 3$ MHz in steps of 50 Hz, BW 10 kHz.

6 Conclusion

In many cases the proposed solution represents an economic, fast and high resolution phase measurement for heterodyne interferometers. Besides its simplicity the presented approach has also the disadvantage of a beat frequency dependent resolution. At certain specific speed values lower resolutions have to be accepted. This approach is certainly not ideal when highly secure and safe systems must be built. Monitoring the beat frequency and a reliable simulation helps to find optimal operating settings. Turbulences, noise and signal jitter can further reduce this effect. In future, with faster and still economic FPGA boards, this approach will gain in attractiveness. The system was implemented in the METAS photomask measuring machine and is now running several months continuously without any interrupts.

References

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